

Slots on boards: Tame them with vias

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Introduction:

Most PCBs designed today have planes for power supplies and ground returns. While most designs try and designate separate layers in the PCB stack-up for power and ground, some high density PCBs go with the idea of a split planes and sharing one physical copper layer across many different power supplies and ground returns. This idea invariably creates reference discontinuities for signals that travel across the length of the PCB making them run over many of these split planes. The straight forward result of this being the increase in return path length and loop area. And as we know, increase in loop area directly translates to increase in EMC issues. So how do we tackle this age old problem of discontinuities in return paths (referred to as “Slots”) in PCB designs without causing any major impact to cost?

A Slotted PCB:

Before proceeding on an expedition to source an idea to solve issues caused by slots on PCBs we need to understand the actual impact a slot creates. To do this, I created a simple 4 layer PCB design in CST Microwave studio and constructed a microstrip trace with 50 ohm characteristic impedance (figure 1).

I simulated the trace with a discontinuity on its return path using a transient solver. The slot area was around 81mm², though in this article, I do not propose to discuss to relate slot area with

performance using numerical values. Instead, I plan to iterate the simple method of using vias can indeed eliminate the fear of using slots.

Surface current on a slotted PCB:

To understand why slots should not be used, we need to have a look at the path the current flows on the trace and its return. As can be seen in figure 2, the current has to go around the slot, in order to return back to the source.

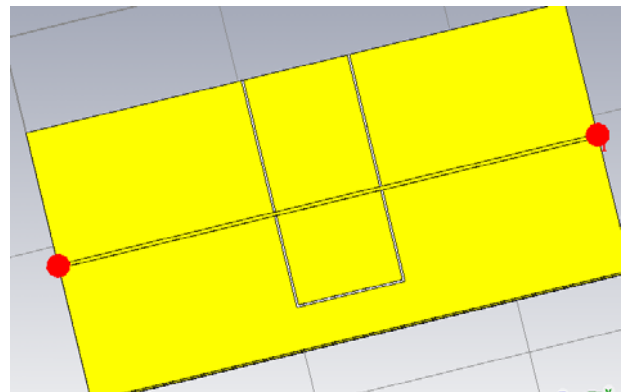
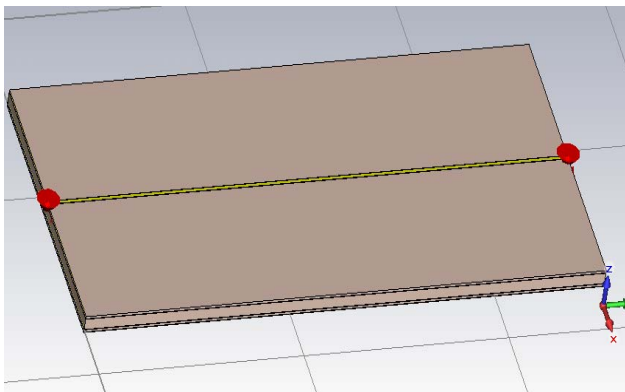


Figure 1: A PCB with slotted ground plane

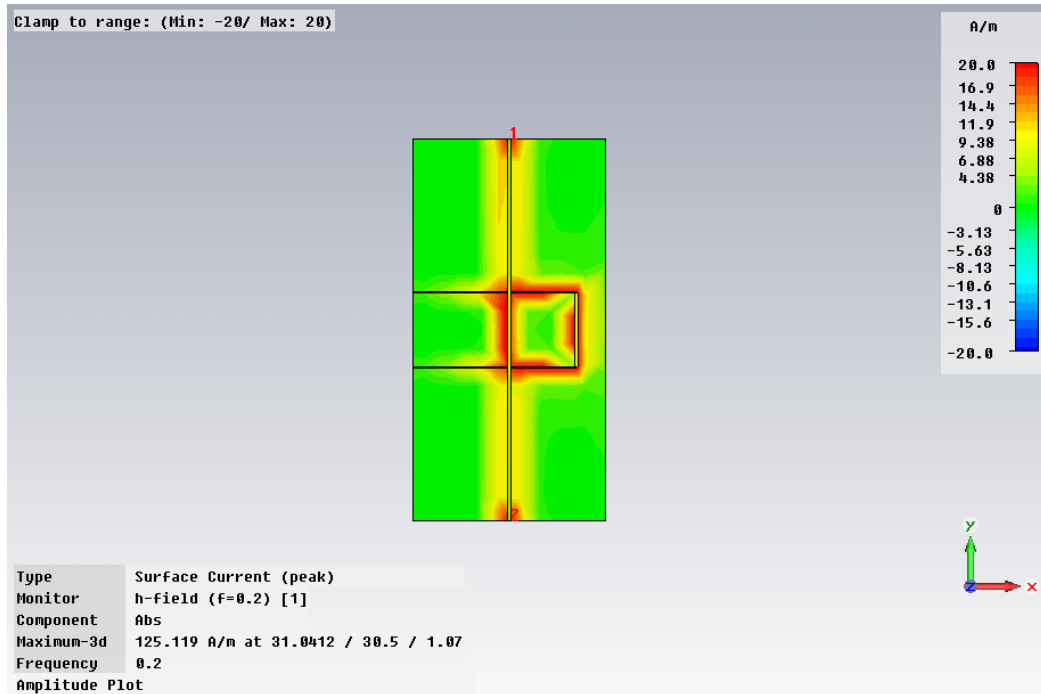


Figure 2: Current path on a slotted PCB (Top View)

Stitching Vias:

The reason behind the current loop in a slotted PCB is the fact that the slot creates a much longer “shortest” current return path. The most intuitive way to reduce this long return path is to drill vias near the slots so that the return current can jump to

the next possible ground layer, if that offers lower impedance. So I added 8 vias to stitch the slotted ground plane with the next plane (that lies 1.0 mm below) and simulated the PCB once again.

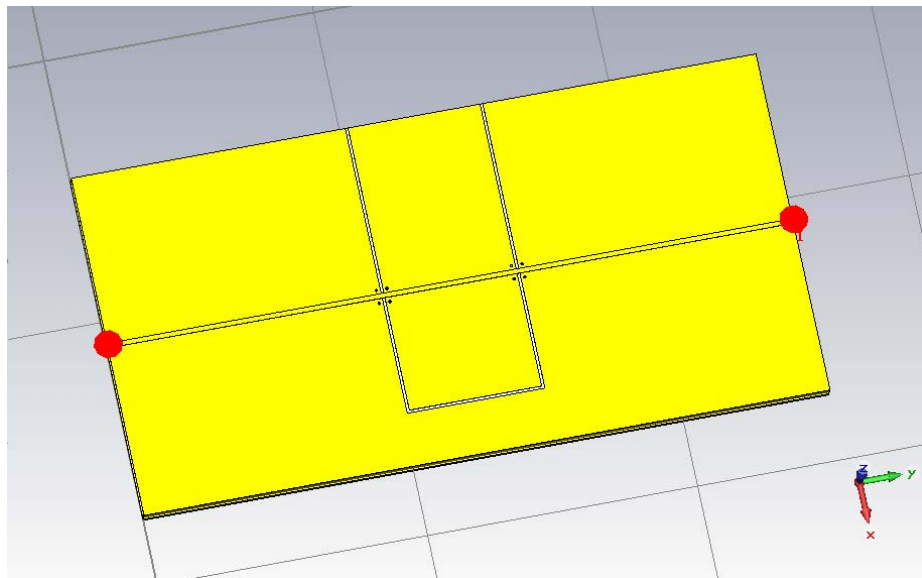


Figure 3: A PCB with slotted ground plans stitched with vias to adjacent plane

Performance Impact:

The adding of stitching vias had an immediate effect on the current paths as the vias now provide a much lower impedance path when compared to before. The absolute value of surface current (figure 4) itself was lower than in the model that had no vias.

EMC Performance:

It was very interesting to see the e-field calculated at 10m distance get much better, once the vias were added (figure 5). By moving the vias farther away from the slots, I was able to make the benefit achieved, worse.

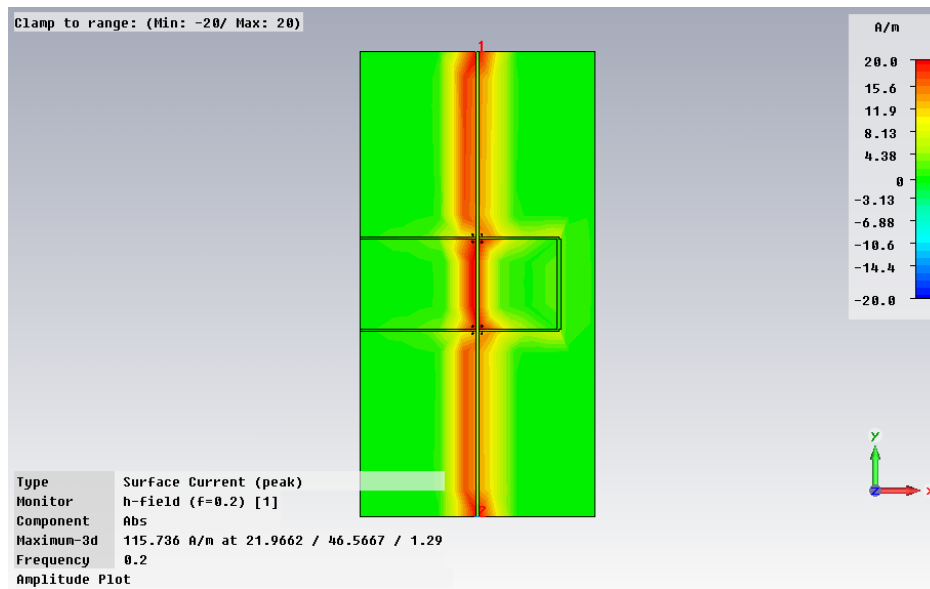


Figure 4: Current path on a slotted PCB with vias (Top)

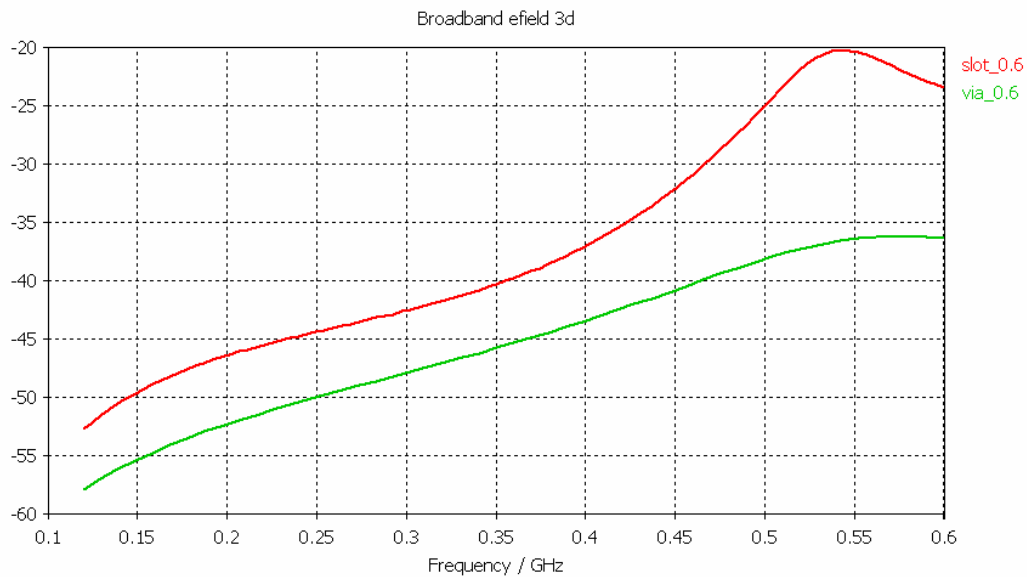


Figure 5: Calculated E-field at 10m.

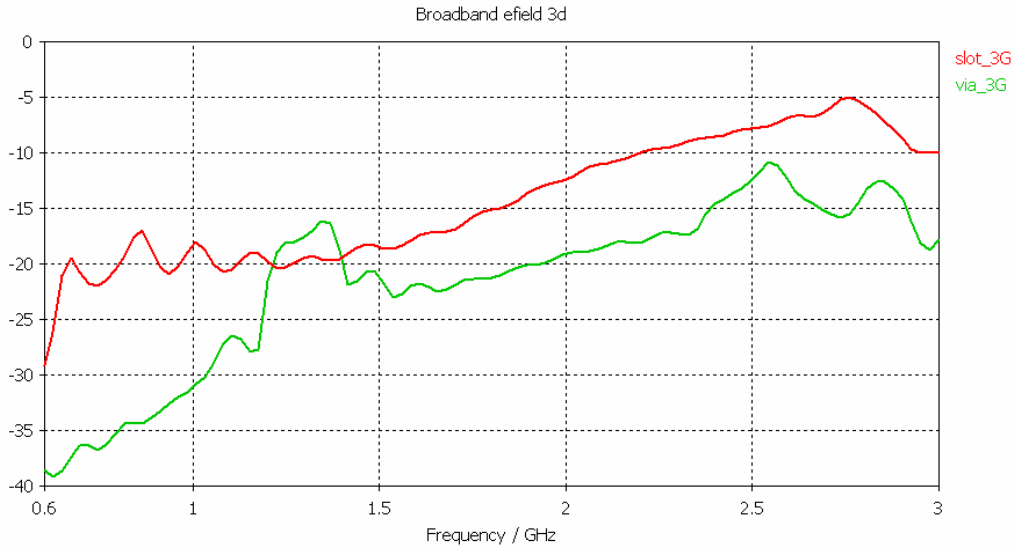


Figure 6: Calculated E-field at 10m

Conclusion:

This shows that the stitching vias offer a fundamental boost to the EMC performance by reducing the loop area. The result was much similar at higher frequencies (figure 6), although I was able to see a particular frequency range (around 1.25GHz) where the trace dimension forms a resonance and the e-field emission increased. But overall, the vias helped in improving the EMC performance.

It is very clear from the above results that adding stitching vias is a very simple and an effective way to handle EMC issues caused by slots. The major challenge however is to be aware of the presence of slots in actual designs that have 10 or 12 layers and has thousands of signal traces. Though it takes time and patience to work out the return path for all the important signals and identify the discontinuities in their return path, it definitely is worth it.