

# Via antipads: How much care do they need?

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## Abstract:

When dealing with high speed designs, electronics engineers tend to match trace impedances to the utmost level possible. They take care of ground returns and crosstalk and try to minimise EMC while maximising Signal Integrity. Though with the increase in PCB complexity, this happens to be a challenge, they try and sacrifice many other parameters to achieve EMC and SI. But, there is one aspect that most engineers overlook – the drilling of Vias. Vias, at very high frequencies behave very differently because their capacitance and inductance appear to matter and start impacting the amount of energy transferred. Does this mean we should not use vias at all at high frequencies? Not necessarily. But we need to design vias with equal care like the traces that connect to the vias. The impedance posed by a via is of equal importance as the trace impedance itself in order to maximise energy transfer.

## Via Structure:

Vias are simple structures that travel from one copper layer to another helping the traces to carry current from one point to another. They are generally drilled and not filled with anything (though high end designs tend to fill these vias tolerating an additional cost). The via structure looks as shown in figure 1 when looked through a PCB. All unfilled vias have a drill hole and plating. A drill hole is the finished size of the via hole after it is plated. The vias

also have a parameter called clearance or antipads. The antipads are nothing but spacing between the via plating and the connection to the adjacent structure. In figure 2, via clearance is the gap between the via plating and the surrounding ground layer. By changing the antipad dimensions we can change the capacitance associated with a via and hence directly control its impedance.

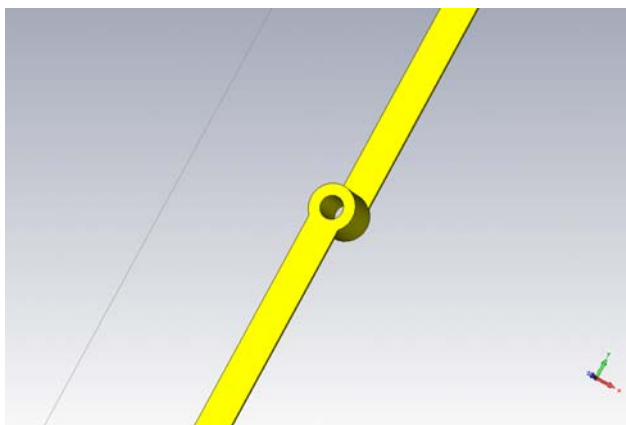


Figure 1: Via Structure

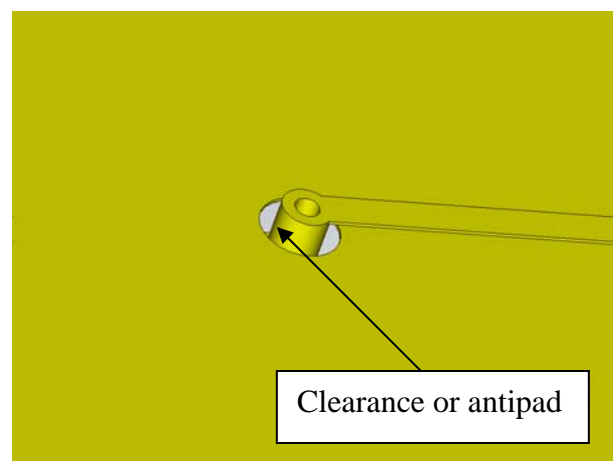
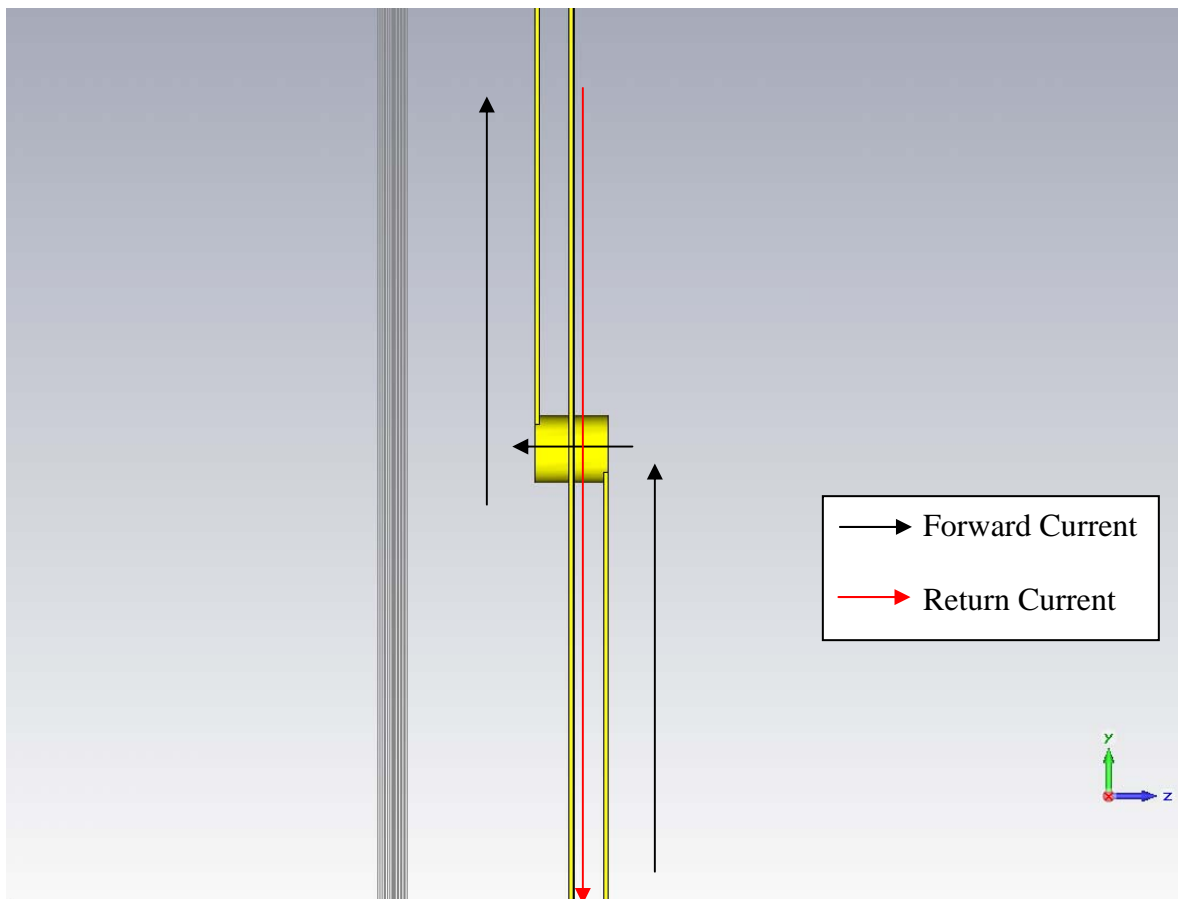


Figure 2: Clearance Pads

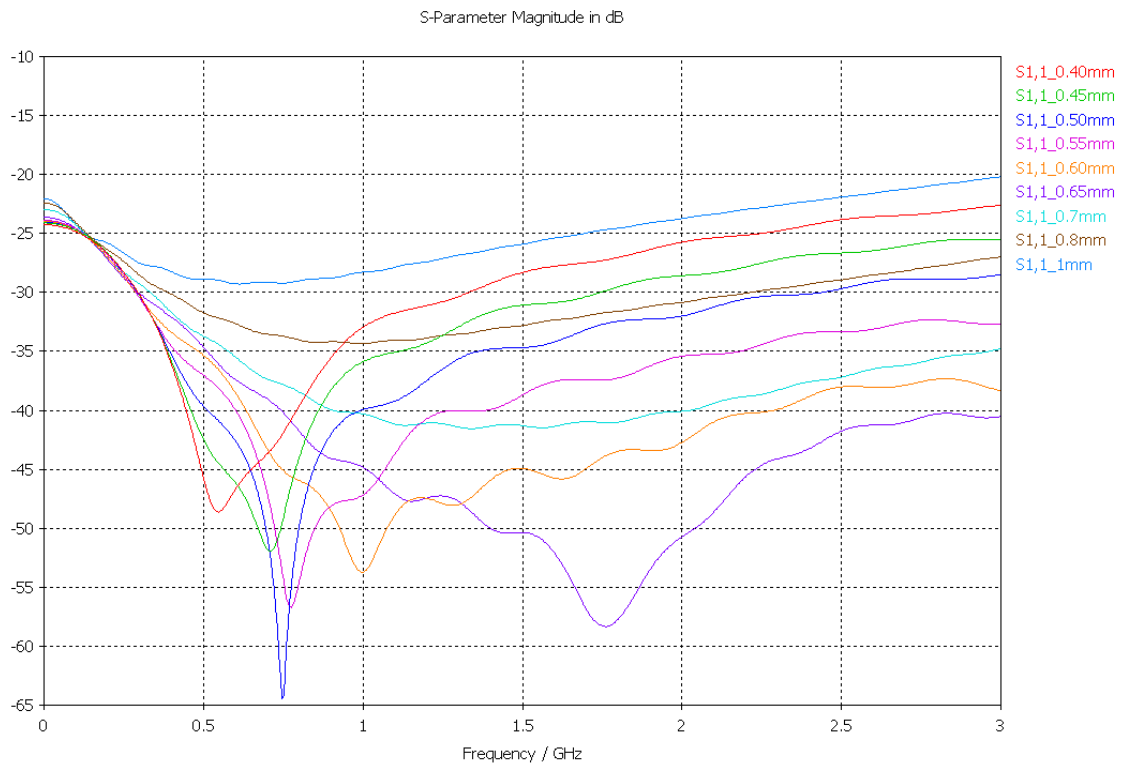
## The importance of antipads:

Until we simulate the via structure along with its return path in a 3D solver, it is very difficult to understand the importance of antipads dimensions. But to gather a basic understanding of the fact that antipads dimensions indeed affect energy transfer, I constructed a simple 3 layer board with a trace running from layer 1 to layer 3. The return current flows in the same plane in layer 2 as shown in Figure 3. The via that connects the trace in layer 1 to the trace in layer 3 is designed with varying antipad dimensions with radius ranging from 0.4mm clearance to 1.00mm. The trace impedances are designed for constant 50 ohms.

Figure 4 shows various antipads dimensions of this single via structure and the  $S_{1,1}$  parameter for these dimensions over frequency. As you can see without really changing any other parameter, we are able to affect  $S_{1,1}$  by 20dB at some higher frequencies. This is because of effect of via capacitance and inductance. In order to have least effect of the via, ideally we need to match the via impedance with the trace impedance.



**Figure 3: Model Construction**



**Figure 4: S1, 1 with varying clearance values**

### Theoretical Calculation:

For simple structures of this sort, that generally have a return path running underneath the structure, we do not always need to simulate the structure. Instead, some theoretical analysis can be done to identify, if maximum energy can be transferred or not. As mentioned before, by varying antipads dimensions, we can match impedance of the via to the trace impedance. (While via drill size can have dramatic effect on impedance, I am going to maintain the via drill size a constant and change antipads dimensions, since this does not have any consequence on cost.)

Inductance of a via:  $L_v = 2L\mu_0 * \ln(b/a)$

$$\text{Capacitance of a via: } C_v = \frac{2\pi\epsilon_0}{\ln(b/a)}$$

Where,

L = Length of the via

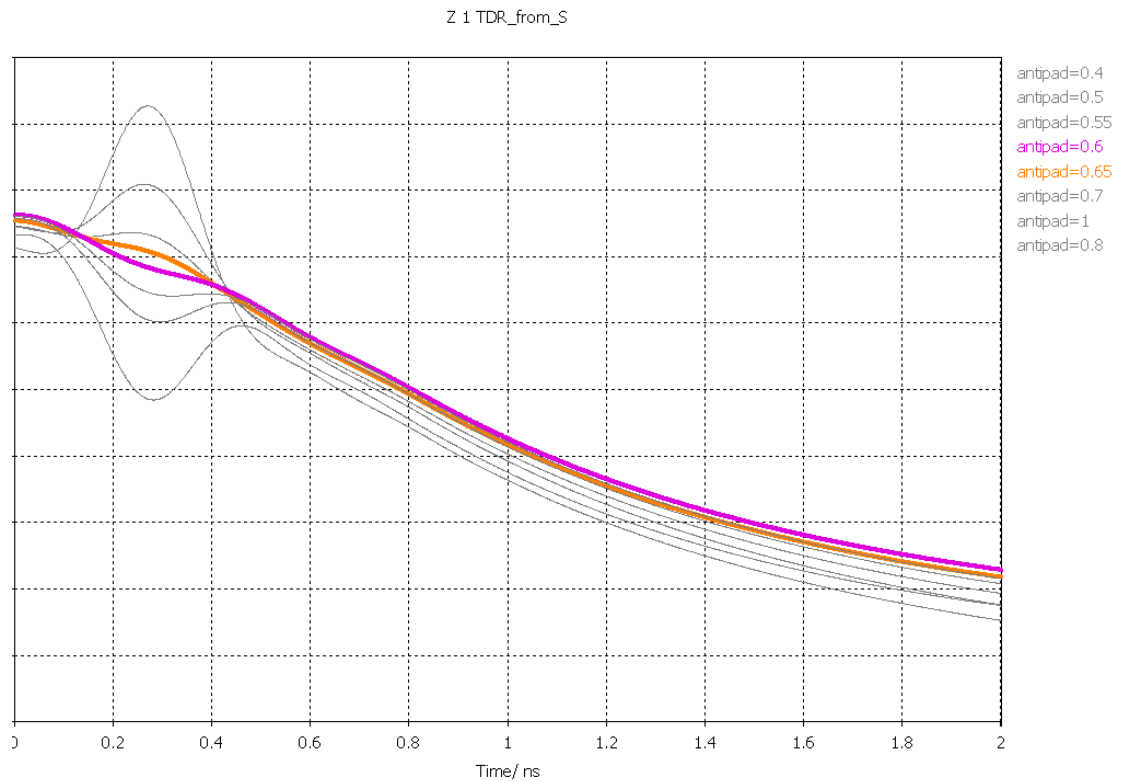
b = clearance diameter

a = Via diameter

Based on these above formulas, we could come up with the following table that would show us varying via impedances for varying antipads dimensions. The Theoretical values predict that the antipad radius of 0.6mm or 0.65mm (diameter of 1.2mm and 1.3mm) would provide the best possible S1, 1. This claim can be verified by a TDR computation on the simulation model which is presented in Figure 5.

Antipad Radius	capacitance in fF	Inductance(fH)	Z(ohms)
0.4	56.19565383	75553.04268	36.66694
0.45	44.93494464	75553.04268	41.00472
0.5	38.10469405	75553.04268	44.52836
0.55	33.49852836	75553.04268	47.4912
0.6	30.16916553	75553.04268	50.04311
0.65	27.64190988	75553.04268	52.28077
0.7	25.65235349	75553.04268	54.27032
0.8	22.70742627	75553.04268	57.68223
1	19.05234703	75553.04268	62.97262

**Table 1: Theoretical calculation of impedance**



**Figure 5: TDR with varying clearance values**

## Conclusion:

It is a good idea to consider varying antipad dimensions for vias that are located on critical traces when the frequencies of interest are higher. A simple structure like this has the best impedance match when the antipad radius is 0.6mm to 0.65mm and that can be seen in the S-parameter results and the TDR results.

Theoretically, for a simple design that has the return path underneath the trace, the via impedance can be calculated on a black board and as it can be seen it closely matches with the simulated results. But for more complex PCBs, it is best to import the design into a 3D solver and work with all the possible return paths for the trace in order to achieve the most realistic results.